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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
GEIB, BENJAMIN P	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 03/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/724,874	AKKARY ET AL.	
	Examiner	Art Unit	
	Benjamin P. Geib	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2003 and 20 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Supervisory

FRITZ FLEMING
PRIMARY EXAMINER
GROUP 2100
AU 2181
3/20/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/20/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-24 have been examined.

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Application on 12/02/2003, Declaration and Information Disclosure Statement on 04/20/2004, and Change of Address on 09/20/2005.

Claim Objections

3. Claim 17 is objected to because of the following informalities: One of the phrases "a branch predictor to" should be deleted from the limitation "a branch predictor to a branch predictor to generate a checkpoint". Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Cristal et al., "Large Virtual ROBs by Processor Checkpointing", (Herein referred to as Cristal).

6. Referring to claim 1, Cristal has taught a method, comprising:

generating a checkpoint *[Cristal; checkpoint entry (CHKPT); page 5, 3rd paragraph]*, wherein said checkpoint is associated with at least one physical register *[A checkpoint is generated that contains a register map table mapping physical registers to*

logical registers (Cristal; page 5, 3rd and 4th paragraphs)], and wherein said at least one physical register is associated with at least one counter *[A counter of the Release Counter Vector (RCV), which contains a counter for each physical register (Cristal; page 4, 8th paragraph)]*

maintaining said at least one physical register until said checkpoint is retired, wherein said at least one physical register is mapped to a logical register *[The checkpoint table maintains physical registers by storing a map table indicating the physical registers mapped to logical registers for the instructions associated with the checkpoint. (Cristal; page 7, 1st paragraph)]*;

updating said at least one counter when one or more instructions are mapped to said logical register *[When an instruction is released from the reorder buffer (ROB) without finishing, the RCV counters RCV(fj_c) and RCV(fk_c) are incremented (i.e. updated). At this point in time an instruction is mapped to the logical register (Cristal; page 8, 1st paragraph)]*;

retiring said checkpoint when all of said one or more instructions associated with said checkpoint have completely executed *[A checkpoint entry is cleared (i.e. the checkpoint is retired) when the last instruction associated with the checkpoint finishes (i.e. has completely executed) (Cristal; page 9, 3rd paragraph)]*; and

releasing said at least one physical register associated with said checkpoint *[Cristal; page 12, 1st – 3rd paragraphs]*.

7. Referring to claim 2, Cristal has taught the method of claim 1, said updating said at least one counter further comprising: incrementing said at least one counter when at

least one instruction with said logical register as an input operand is renamed to said at least one physical register *[When an instruction is released from the reorder buffer (ROB) without finishing, the RCV counters RCV(fj_c) and RCV(fk_c) are incremented. At this point in time the instruction with a logical register as an input operand has been renamed to a physical register (Cristal; page 8, 1st paragraph)]*.

8. Referring to claim 3, Cristal has taught the method of claim 2, said updating said at least one counter further comprising: decrementing said at least one counter when said instruction is issued and reads said at least one physical register *[When an instruction is finished the RCV counters RCV(fi) and RCV(fk_c) are decremented. At this point in time, the instruction has been issued and read at least one physical register (Cristal; page 9, 2nd paragraph)]*.

9. Referring to claim 4, Cristal has taught the method of claim 1, said releasing said at least one physical register further comprising: releasing said at least one physical register when said counter is decremented, wherein said decrementing reaches a state indicating that none of said instructions have yet to read said at least one physical register *[The physical register is released when its RCV counter is equal to zero (Cristal; page 12 3rd paragraph), which indicates that there are no more instructions that have yet to read from the physical register (Cristal; page 4, 8th paragraph)]*.

10. Referring to claim 5, Cristal has taught the method of claim 4, said releasing said at least one physical register further comprising: releasing said at least one physical register only after said associated checkpoint is released *[When a checkpoint entry is*

clear (i.e. the checkpoint is released), RCV counters RCV(fi) and RCV(fk_c) are decremented and equal zero (Cristal; page 9, 3rd paragraph). When an RCV counter is equal to zero, the physical register associated with the counter is released (Cristal; page 12, 3rd paragraph)].

11. Referring to claim 6, Cristal has taught the method of claim 1, wherein said checkpoint includes at least one unmapped flag for each of said at least one physical register associated with said checkpoint *[The checkpoint includes the commit mapping table (CHKPT-CMT; See Fig. 7) which comprises an unmapped flag for each physical register. (Cristal; page 4, 2nd paragraph; page 7, 1st paragraph)].*

12. Referring to claim 7, Cristal has taught the method of claim 1, wherein said at least one counter is incremented when said checkpoint is generated *[The RCV counters RCV(fj_c) and RCV(fk_c) are incremented when a checkpoint is created; (Cristal; page 8, 1st paragraph)].*

13. Referring to claim 8, Cristal has taught the method of claim 1, wherein said at least one counter is decremented when said checkpoint is retired *[The RCV counters RCV(fi) and RCV(fk_c) are decremented when a checkpoint entry is cleared (i.e. retired); (Cristal; page 9, 3rd paragraph)].*

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 9-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cristal in view of Moshovos, "Checkpointing Alternatives for High Performance, Power-Aware Processors".

16. Referring to claim 9, Cristal has taught an apparatus, comprising:

a checkpoint generator *[The inherent circuitry required to perform the described checkpointing]* to generate a checkpoint *[Cristal; checkpoint entry (CHKPT); page 5, 3rd paragraph]*, wherein said checkpoint is associated with at least one physical register *[A checkpoint is generated that contains a register map table mapping physical registers to logical registers (Cristal; page 5, 3rd and 4th paragraphs)]*;

a checkpoint buffer *[Cristal; checkpoint table (CT); page 5, 3rd paragraph]* to maintain said at least one physical register, said at least one physical register associated with one or more instructions *[The checkpoint table maintains physical registers by storing a map table indicating physical register allocations for the instructions associated with the checkpoint. (Cristal; page 7, 1st paragraph)]*;

wherein said checkpoint generator retires said checkpoint when all of said one or more instructions have completely executed *[A checkpoint entry is cleared (i.e. the checkpoint is retired) when the last instruction associated with the checkpoint finishes (i.e. has completely executed) (Cristal; page 9, 3rd paragraph)]* and releases said at least one physical register associated with said checkpoint *[Cristal; page 12, 1st – 3rd paragraphs]*.

Cristal has not explicitly taught that a branch predictor generates the checkpoint.

Moshovos has taught a branch predictor that generates checkpoints *[Moshovos; page 3, column 1]*.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the checkpoint generator of Cristal to be a branch predictor as taught by Moshovos.

The suggestion/motivation for doing so would have been that doing so offers "most of performance advantages of RAT checkpointing with much lower resources and power" *[Moshovos; page 2, column 2, 1st paragraph]*.

Therefore, it would have been obvious to combine Moshovos with Cristal to obtain the invention as specified in claim 9.

17. Referring to claim 10, has taught the apparatus of claim 9, wherein said checkpoint buffer increments at least one counter *[a counter of the Release Counter Vector (RCV)]* when said checkpoint is generated *[The RCV counters RCV(fj_c) and RCV(fk_c) are incremented when a checkpoint is created; (Cristal; page 8, 1st paragraph)]*; wherein said at least one counter is associated with said at least one physical register *[The incremented RCV counters correspond to the physical registers allocated to the logical registers associated with the current instruction (Cristal; page 4, 5th and 8th paragraphs)]*.

18. Referring to claim 11, has taught the apparatus of claim 9, wherein said checkpoint buffer decrements at least one counter when said checkpoint is retired *[The*

RCV counters RCV(fi) and RCV(fk_c) are decremented when a checkpoint entry is cleared; (Cristal; page 9, 3rd paragraph)], wherein said at least one counter is associated with said at least one physical register *[The decremented RCV counters correspond to the physical registers allocated to the logical registers associated with the current instruction (Cristal; page 4, 5th and 8th paragraphs)]*.

19. Referring to claim 12, has taught the apparatus of claim 9, wherein said branch predictor increments at least one counter when at least one of said one or more instructions with a logical register as an input operand is renamed to said at least one physical register *[When an instruction is released from the reorder buffer (ROB) without finishing, the RCV counters RCV(fj_c) and RCV(fk_c) are incremented. At this point in time the instruction with a logical register as an input operand has been renamed (Cristal; page 8, 1st paragraph)]*.

20. Referring to claim 13, has taught the apparatus of claim 9, wherein said branch predictor decrements at least one counter when at least one of said one or more instructions is issued and reads said at least one physical register *[When an instruction is finished the RCV counters RCV(fi) and RCV(fk_c) are decremented. At this point in time, the instruction has been issued and read at least one physical register (Cristal; page 9, 2nd paragraph)]*.

21. Referring to claim 14, has taught the apparatus of claim 9, wherein said branch predictor releases said at least one physical register when at least one counter *[RCV(f) counter]* is decremented to a state *[RCV(f) =0]* indicating that none of said one or more instructions have yet to read said at least one physical register *[The physical register is*

released when its RCV counter is equal to zero (Cristal; page 12 3rd paragraph), which indicates that there are no more instructions that have yet to read from the physical register (Cristal; page 4, 8th paragraph)].

22. Referring to claim 15, has taught the apparatus of claim 14, wherein said branch predictor releases said at least one physical register after said checkpoint is released *[When a checkpoint entry is clear (i.e. the checkpoint is released), RCV counters RCV(fi) and RCV(fk_c) are decremented and equal zero (Cristal; page 9, 3rd paragraph). When an RCV counter is equal to zero, the physical register associated with the counter is released (Cristal; page 12, 3rd paragraph)].*

23. Referring to claim 16, has taught the apparatus of claim 9, wherein said checkpoint includes at least one unmapped flag for each of said at least one physical registers associated with said checkpoint *[The checkpoint includes the commit mapping table (CHKPT-CMT; See Fig. 7) which comprises an unmapped flag for each physical register. (Cristal; page 4, 2nd paragraph; page 7, 1st paragraph)].*

24. Referring to claim 17, has taught a system, comprising:

a processor including

a checkpoint generator to generate a checkpoint *[Cristal; checkpoint entry (CHKPT); page 5, 3rd paragraph]*, wherein said checkpoint is associated with at least one physical register *[A checkpoint is generated that contains a register map table mapping physical registers to logical registers (Cristal; page 5, 3rd and 4th paragraphs)]*;

a checkpoint buffer *[Cristal; checkpoint table (CT); page 5, 3rd paragraph]* to maintain said at least one physical register, said at least one physical register associated with one or more instructions *[The checkpoint table maintains physical registers by storing a map table indicating physical register allocations for the instructions associated with the checkpoint. (Cristal; page 7, 1st paragraph)]*;

wherein said checkpoint generator retires said checkpoint when all of said one or more instructions have completely executed *[A checkpoint entry is cleared (i.e. the checkpoint is retired) when the last instruction associated with the checkpoint finishes (i.e. has completely executed) (Cristal; page 9, 3rd paragraph)]* and releases said at least one physical register associated with said checkpoint *[Cristal; page 12, 1st – 3rd paragraphs]*.

Cristal has not explicitly taught that a branch predictor generates the checkpoint.

Moshovos has taught a branch predictor that generates checkpoints *[Moshovos; page 3, column 1]*.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the checkpoint generator of Cristal to be a branch predictor as taught by Moshovos.

The suggestion/motivation for doing so would have been that doing so offers "most of performance advantages of RAT checkpointing with much lower resources and power" *[Moshovos; page 2, column 2, 1st paragraph]*.

Cristal and Moshovos have not explicitly taught an interface to couple said processor to input-output devices and a data storage coupled to said interface to receive code from said processor.

However, Examiner takes Official Notice that an interface to couple a processor to input-output devices and data storage coupled to the interface to receive code from the processor is a conventional and well-known means of communicating and storing code.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Cristal and Moshovos to include an interface to couple the processor to input-output devices and a data storage coupled to the interface since doing so allows the processor to receive code and store code, as well as communicating with I/O devices as required by the high performance processor of Moshovos.

Therefore, it would have been obvious to combine Moshovos with Cristal to obtain the invention as specified in claim 17.

25. Referring to claim 18, given the similarities between claim 10 and claim 18 the arguments as stated for the rejection of claim 10 also apply to claim 18.

26. Referring to claim 19, given the similarities between claim 11 and claim 19 the arguments as stated for the rejection of claim 11 also apply to claim 19.

27. Referring to claim 20, given the similarities between claim 12 and claim 20 the arguments as stated for the rejection of claim 12 also apply to claim 20.

28. Referring to claim 21, given the similarities between claim 13 and claim 21 the arguments as stated for the rejection of claim 13 also apply to claim 21.

29. Referring to claim 22, given the similarities between claim 14 and claim 22 the arguments as stated for the rejection of claim 14 also apply to claim 22.

30. Referring to claim 23, given the similarities between claim 15 and claim 23 the arguments as stated for the rejection of claim 15 also apply to claim 23.

31. Referring to claim 24, given the similarities between claim 16 and claim 24 the arguments as stated for the rejection of claim 16 also apply to claim 24.

Conclusion

32. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

33. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tovey et al., U.S. Patent No. 5,740,414, teaches a system for coordinating physical register usage in a processor using checkpoints.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Benjamin P Geib
Examiner
Art Unit 2181

Supervisory

FRITZ FLEMING
PRIMARY EXAMINER
GROUP 2100
AU 2181 3/10/2006